In the Claims:

1. (Currently Amended) A field effect transistor comprising:

a fin extending from a substrate, the fin including an upper portion remote from the substrate and opposing sidewalls that extend between the upper portion and the substrate;

a channel region in the fin;

a gate electrode adjacent the channel region and crossing over the fin;

a gate insulation layer interposed between the gate electrode and the fin;

source/drain regions formed at both sides of the gate electrode, wherein the channel region at the upper portion of the fin is doped higher than sidewalls of the fin;

a device isolation layer on the substrate including respective portions that extend to a respective opposing sidewall of the fin to define an opening in the device isolation layer; and

a punch-through stop layer **[[in]]** that is confined to within the opening between the portions of the device isolation layer, the punch-through stop layer having a higher doping concentration than the sidewalls of the fin in the channel region.

2. (Original) The transistor of Claim 1, wherein the channel region comprises:

a first layer in the upper portion of the fin; and

a second layer beneath the first layer, wherein the second layer is lightly doped relative to the first layer.

3. (Canceled)

4. (Original) The transistor of Claim 1:

wherein the substrate is a bulk semiconductor layer; and

wherein the semiconductor layer extends vertically to form the fin.

5. (Original) The transistor of Claim 4, further comprising an insulation layer disposed between the gate electrode and the semiconductor layer at a periphery of the fin.

6. (Previously Presented) The transistor of Claim 2, wherein the punch-through stop layer has a higher doping concentration than the second layer.

7. (Original) The transistor of Claim 2, wherein the second layer has uniform concentration in the channel region.

8-12. (Canceled)

13. (Currently Amended) An integrated circuit field effect transistor comprising:

an integrated circuit substrate;

a fin that projects away from the integrated circuit substrate, extends along the integrated circuit substrate and includes a top that is remote from the integrated circuit substrate and opposing sidewalls that extend between the top and the integrated circuit substrate;

a channel region in the fin that is doped a predetermined conductivity type and having a higher doping concentration of the predetermined conductivity type adjacent the top than remote from the top;

a source region and a drain region in the fin on respective opposite sides of the channel region;

an insulated gate electrode that extends across the fin, adjacent the channel region;

a device isolation layer on the integrated circuit substrate including respective portions that extend to a respective opposing sidewall of the fin to define an opening in the device isolation layer; and

a punch-through stop layer [[in]] <u>that is confined to within</u> the opening between the portions of the device isolation layer, the punch-through stop layer

having a higher doping concentration of the predetermined conductivity type than the channel region remote from the top.

14. (Original) The integrated circuit field effect transistor according to Claim 13 wherein the channel region is uniformly doped the predetermined conductivity type at a first doping concentration except for being doped the predetermined conductivity type at a second doping concentration that is higher than the first doping concentration adjacent the top.

15. (Original) The integrated circuit field effect transistor according to Claim 13 wherein the channel region comprises a first region of the predetermined conductivity type adjacent the top and a second region of the predetermined conductivity type remote from the top, wherein the first region is more heavily doped than the second region.

16. (Previously Presented) The integrated circuit field effect transistor according to Claim 13 wherein the channel region has the higher doping concentration of the predetermined conductivity type directly beneath the top, from one of the opposing sidewalls to the other of the opposing sidewalls.

17. (Original) The integrated circuit field effect transistor according to Claim 13:

wherein the integrated circuit substrate is a bulk semiconductor substrate such that the bulk semiconductor substrate includes a projection that defines the fin;

the integrated circuit field effect transistor further comprising a region of the predetermined conductivity type in the bulk semiconductor substrate beneath the fin.

18. (Canceled)

19. (Original) The integrated circuit field effect transistor according to Claim 13 further comprising:

a capacitor connected to the source region.

20. (Original) The integrated circuit field effect transistor according to Claim 13 further comprising:

a bit line connected to the drain region.

21-22. (Canceled)